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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,806	02/10/2004	Alexander Kushnarenko	P-6274-US	9248

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EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,806	KUSHNARENKO, ALEXANDER	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,11-15 and 17 is/are rejected.

7)☒ Claim(s) 2-10 and 16 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 10 February 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/18/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 4-6 are objected to because of the following informalities:

In claims 4 and 6, line 2, after "inverted switch", -- . – should be inserted.

In claim 5, line 3, after "input node", -- . – should be inserted.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

Claims 11 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 11, the limitation "low voltage source is charged during a discharge of said power driver circuit" is not clearly defined. How does the "low voltage source is charged during a discharge" occurs? In order to avoid any confusion, Applicant is required to particularly point out how this limitation reads on the circuit arrangement of the drawings.

In claim 15, the limitation "...connecting said output node to said low voltage source" is misdescriptive of the present invention since such limitation is not seen as recited therein. In order to avoid any confusion, Applicant is required to particularly point out how this limitation reads on the circuit arrangement of the drawings. Is applicant meant "connecting said output node to said high voltage source"?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 11-15 are rejected under 35 U.S.C. 102(b) as being anticipated by the prior art depicted by Applicant's Fig. 2.

The prior art, Fig. 2 disclosed a conventional high voltage driver with Vcc pre-charge including:

a low voltage source (Vcc);

a high voltage source (HV);

a first input node (IN1-P);

an output node (nOUT); and

circuitry (PO, NO, N1) adapted to connect said output node (nOUT) to said low voltage source (Vcc) when a signal at said first input node is in a first state (when IN1-P is HIGH, IN2 IS LOW, connected to Vcc) and to said high voltage source (HV) when said signal at said first input node is changed to a second state (when IN1-P is LOW, PO is ON, IN2 is either HIGH or LOW, connected to HV) and recited in claim 1.

Regarding claim 11, due to indefiniteness, the limitation "low voltage source is charged during a discharge" can not given sufficient weight to read over the reference. Element Vcc reads on the low voltage source.

Regarding claim 12, low voltage source is Vcc (Vcc).

The method recited in claim 13 is similarly rejected as claim 1: connecting said output node (Nout) to said low voltage source (Vcc) when a signal at a first input node is in a first state (when IN1-P is HIGH, IN2 IS LOW, connected to Vcc) and to said high voltage source (HV) when a signal at said first input node is changed to a second state (when IN1-P is LOW, PO is ON, IN2 is either HIGH or LOW, connected to HV).

Regarding claim 14: said connecting said output node to said high voltage source when a signal at said first input node is in said second state comprises providing a high voltage on signal at said first input node to a switch connecting said output node to said low voltage source (when IN1-P is HIGH, IN2 is LOW, connected to Vcc).

Regarding claim 15: said connecting said output node to said low voltage source when a signal at said first input node is in said first state comprises providing a low voltage off signal at said first input node to a switch connecting said output node to said low voltage source (due to indefiniteness, the limitation "low voltage source" can not given sufficient weight to read over the reference. Clearly, when IN1-P is LOW, PO is ON, connected to HV).

Claims 1, 11-13, 15 and 17 are also rejected under 35 U.S.C. 102(b) as being anticipated by Shin et al (U.S. Patent No. 4,733,105).

Shin et al disclosed a CMOS output circuit including:

a low voltage source (V1);

a high voltage source (VDD);

a first input node (S11);

an output node (node connected between 33, 56 and 38, connect to A); and

circuitry (31, 32, 52, 33, 56) adapted to connect said output node (the node connected between 33, 56 and 38, connect to A) to said low voltage source (V1) when a signal at said first input node is in a first state and to said high voltage source (VDD) when said signal at said first input node is changed to a second state (when S11 is LOW, 31a & 32 ON, connected to V1, and when S11 is changed to HIGH, connected to VDD) and recited in claim 1.

Regarding claim 11, due to indefiniteness, the limitation "low voltage source is charged during a discharge" can not given sufficient weight to read over the reference. Element V1 reads on the low voltage source.

Regarding claim 12, low voltage source is Vcc (seen as V1).

The method recited in claim 13 is similarly rejected as claim 1: connecting said output node to said low voltage source (V1) when a signal at a first input node is in a first state and to said high voltage source (VDD) when a signal at said first input node is changed to a second state (when S11 is LOW, 31a & 32 ON, connected to V1, and when S11 is changed to HIGH, connected to VDD).

Regarding claim 15: connecting the output node to the low voltage source when a signal at the first input node is in the first state comprises providing a low voltage off signal at the first input node to a switch connecting the output node to the low voltage source (when S11 is LOW, 31a & 32 ON, connected to V1).

Regarding claim 17: connecting the output node to the low voltage source (when S11 is LOW) after disconnecting the output node from the high voltage source (S11 remains LOW), thereby charging the low voltage source (charging V1).

Allowable Subject Matter

Claims 2-10, 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: the combination of "low voltage switching circuitry", "high voltage switching circuitry" and "ground switching circuitry" as recited in claim 2; "connecting said output node to ground ... is changed from a first state to a second state" as recited in claim 16.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton

MY-TRANG NU TON
PRIMARY EXAMINER
5/19/05